Lead-Free Package Options Available!

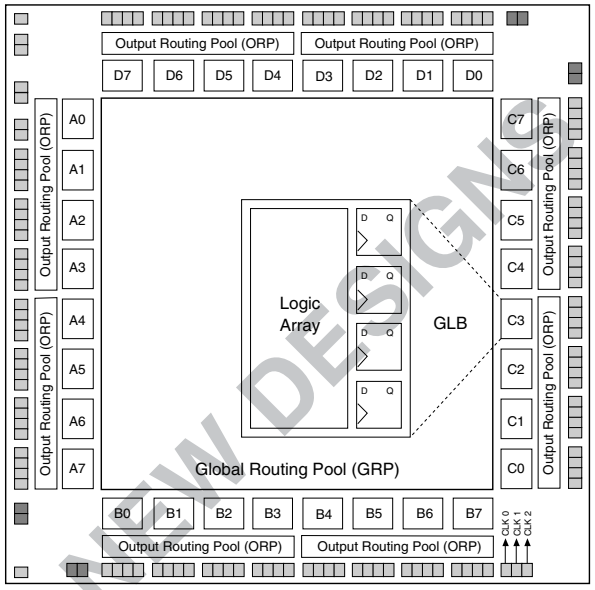
ispLSI® 2128/A

In-System Programmable High Density PLD

Features

- **ENHANCEMENTS**
  - — ispLSI 2128A is Fully Form and Function Compatible to the ispLSI 2128, with Identical Timing Specifcations and Packaging
  - — ispLSI 2128A is Built on an Advanced 0.35 Micron E²CMOS® Technology
- **HIGH DENSITY PROGRAMMABLE LOGIC**
  - — 6000 PLD Gates
  - — 128 I/O Pins, Eight Dedicated Inputs
  - — 128 Registers
  - — High Speed Global Interconnect
  - — Wide Input Gating for Fast Counters, State Machines, Address Decoders, etc.
  - — Small Logic Block Size for Random Logic
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - — f_{max} = 100 MHz Maximum Operating Frequency
  - — t_{pd} = 10 ns Propagation Delay
  - — TTL Compatible Inputs and Outputs
  - — Electrically Erasable and Reprogrammable
  - — Non-Volatile
  - — 100% Tested at Time of Manufacture
  - — Unused Product Term Shutdown Saves Power
- **IN-SYSTEM PROGRAMMABLE**
  - — In-System Programmable (ISP™) 5V Only
  - — Increased Manufacturing Yields, Reduced Time-to-Market and Improved Product Quality
  - — Reprogram Soldered Devices for Faster Prototyping
- **OFFERS THE EASE OF USE AND FAST SYSTEM SPEED OF PLDs WITH THE DENSITY AND FLEXIBILITY OF FIELD PROGRAMMABLE GATE ARRAYS**
  - — Complete Programmable Device Can Combine Glue Logic and Structured Designs
  - — Enhanced Pin Locking Capability
  - — Three Dedicated Clock Input Pins
  - — Synchronous and Asynchronous Clocks
  - — Programmable Output Slew Rate Control to Minimize Switching Noise
  - — Flexible Pin Placement
  - — Optimized Global Routing Pool Provides Global Interconnectivity
  - — Lead-Free Package Options

Functional Block Diagram



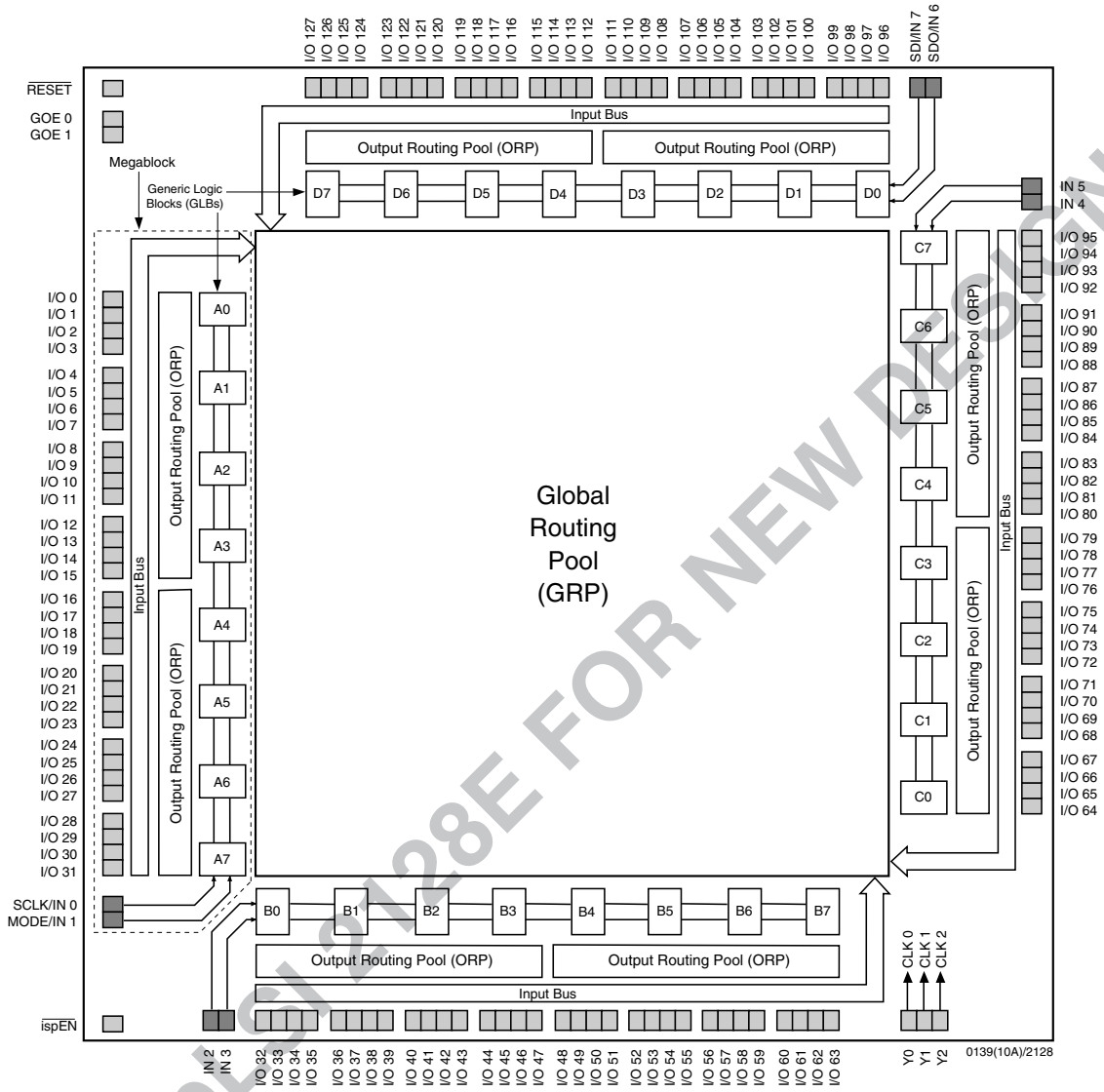
Description

The ispLSI 2128 and 2128A are High Density Programmable Logic Devices. The devices contains128 Registers, 128 Universal I/O pins, eight Dedicated Input pins, three Dedicated Clock Input pins, two dedicated Global OE input pins and a Global Routing Pool (GRP). The GRP provides complete interconnectivity between all of these elements. The ispLSI 2128 and 2128A feature 5V in-system programmability and in-system diagnostic capabilities. The ispLSI 2128 and 2128A offer non-volatile reprogrammability of the logic, as well as the interconnect to provide truly reconfigurable systems.

The basic unit of logic on these devices is the Generic Logic Block (GLB). The GLBs are labeled A0, A1 .. D7 (Figure 1). There are a total of 32 GLBs in the ispLSI 2128 and 2128A devices. Each GLB is made up of four macrocells. Each GLB has 18 inputs, a programmable AND/OR/Exclusive OR array, and four outputs which can be configured to be either combinatorial or registered. Inputs to the GLB come from the GRP and dedicated inputs. All of the GLB outputs are brought back into the GRP so that they can be connected to the inputs of any GLB on the device.

Functional Block Diagram

Figure 1. ispLSI 2128/A Functional Block Diagram



The device also has 128 I/O cells, each of which is directly connected to an I/O pin. Each I/O cell can be individually programmed to be a combinatorial input, output or bi-directional I/O pin with 3-state control. The signal levels are TTL compatible voltages and the output drivers can source 4 mA or sink 8 mA. Each output can be programmed independently for fast or slow output slew rate to minimize overall output switching noise.

Eight GLBs, 32 I/O cells, two dedicated inputs and two ORPs are connected together to make a Megablock (Figure 1). The outputs of the eight GLBs are connected to a set of 32 universal I/O cells by the two ORPs. Each ispLSI 2128 and 2128A device contains four Megablocks.

The GRP has as its inputs, the outputs from all of the GLBs and all of the inputs from the bi-directional I/O cells. All of these signals are made available to the inputs of the GLBs. Delays through the GRP have been equalized to minimize timing skew.

Clocks in the ispLSI 2128 and 2128A devices are selected using the dedicated clock pins. Three dedicated clock pins (Y0, Y1, Y2) or an asynchronous clock can be selected on a GLB basis. The asynchronous or Product Term clock can be generated in any GLB for its own clock.

Absolute Maximum Ratings [1]

Supply Voltage V_{cc} .....-0.5 to +7.0V

Input Voltage Applied..... -2.5 to V_{CC} +1.0V

Off-State Output Voltage Applied ..... -2.5 to V_{CC} +1.0V

Storage Temperature..... -65 to 150°C

Case Temp. with Power Applied ..... -55 to 125°C

Max. Junction Temp. (T_J) with Power Applied ... 150°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

DC Recommended Operating Condition

SYMBOL	PARAMETER			MIN.	MAX.	UNITS
V_{CC}	Supply Voltage	Commercial	T_A = 0°C to + 70°C	4.75	5.25	V
		Industrial	T_A = -40°C to + 85°C	4.5	5.5	V
V_{IL}	Input Low Voltage			0	0.8	V
V_{IH}	Input High Voltage			2.0	V_{CC}+1	V

Table 2 - 0005/2128

Capacitance (T_A=25°C, f=1.0 MHz)

SYMBOL	PARAMETER	TYPICAL	UNITS	TEST CONDITIONS
C_1	I/O and Dedicated Input Capacitance	8	pf	V_{CC}= 5.0V, $V_{I/O, IN}$ = 2.0V
C_2	Clock Capacitance	15	pf	V_{CC}= 5.0V, V_Y= 2.0V

Table 2-0006/2128

Data Retention Specifications

PARAMETER	MINIMUM	MAXIMUM	UNITS
Data Retention	20	–	Years
Erase/Reprogram Cycles	10,000	–	Cycles

Table 2-0008/2128

Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Time	≤ 3ns 10% to 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure 2

3-state levels are measured 0.5V from steady-state active level.

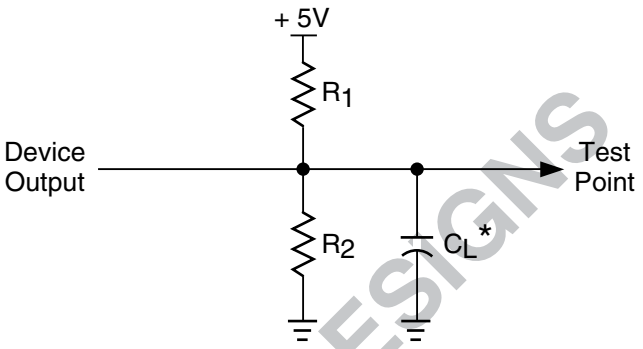
Table 2 - 0003/2000

Output Load Conditions (see Figure 2)

TEST CONDITION		R1	R2	CL
A		470Ω	390Ω	35pF
B	Active High	∞	390Ω	35pF
	Active Low	470Ω	390Ω	35pF
C	Active High to Z at V_{OH} -0.5V	∞	390Ω	5pF
	Active Low to Z at V_{OL} +0.5V	470Ω	390Ω	5pF

Table 2 - 0004A/2000

Figure 2. Test Load



*C_L includes Test Fixture and Probe Capacitance.

0213A

DC Electrical Characteristics

Over Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITION		MIN.	TYP.[3]	MAX.	UNITS
V_{OL}	Output Low Voltage	I_{OL} = 8 mA		–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4	–	–	V
I_{IL}	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (Max.)		–	–	-10	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}		–	–	10	µA
I_{IL-isp}	$\overline{ispEN}$ Input Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{IL-PU}	I/O Active Pull-Up Current	0V ≤ V_{IN} ≤ V_{IL}		–	–	-150	µA
I_{OS}[1]	Output Short Circuit Current	V_{CC} = 5V, V_{OUT} = 0.5V		–	–	-200	mA
I_{CC}[2, 4]	Operating Power Supply Current	V_{IL} = 0.0V, V_{IH} = 3.0V f_{CLOCK} = 1 MHz	Commercial	–	165	325	mA
			Industrial	–	165	–	mA

Table 2-0007/2128

1. One output at a time for a maximum duration of one second. V_{OUT} = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
2. Measured using eight 16-bit counters.
3. Typical values are at V_{CC} = 5V and T_A = 25°C.
4. Maximum I_{CC} varies widely with specific device configuration and operating frequency. Refer to the Power Consumption section of this data sheet and the Thermal Management section of the Lattice Semiconductor Data Book or CD-ROM to estimate maximum I_{CC}.

External Timing Parameters

Over Recommended Operating Conditions

PARAMETER	TEST COND.[4]	#[2]	DESCRIPTION[1]	-100		-80		UNITS
				MIN.	MAX.	MIN.	MAX.	
t_{pd1}	A	1	Data Propagation Delay, 4PT Bypass, ORP Bypass	–	10.0	–	15.0	ns
t_{pd2}	A	2	Data Propagation Delay	–	13.0	–	18.5	ns
f_{max}	A	3	Clock Frequency with Internal Feedback[3]	100	–	81.0	–	MHz
f_{max} (Ext.)	–	4	Clock Frequency with External Feedback $\left(\frac{1}{t_{su2} + t_{co1}}\right)$	77.0	–	57.0	–	MHz
f_{max} (Tog.)	–	5	Clock Frequency, Max. Toggle	100	–	83.0	–	MHz
t_{su1}	–	6	GLB Reg. Setup Time before Clock, 4 PT Bypass	6.5	–	9.0	–	ns
t_{co1}	A	7	GLB Reg. Clock to Output Delay, ORP Bypass	–	5.0	–	6.5	ns
t_{h1}	–	8	GLB Reg. Hold Time after Clock, 4 PT Bypass	0.0	–	0.0	–	ns
t_{su2}	–	9	GLB Reg. Setup Time before Clock	8.0	–	11.0	–	ns
t_{co2}	–	10	GLB Reg. Clock to Output Delay	–	6.0	–	8.0	ns
t_{h2}	–	11	GLB Reg. Hold Time after Clock	0.0	–	0.0	–	ns
t_{r1}	A	12	Ext. Reset Pin to Output Delay	–	13.5	–	17.0	ns
t_{rw1}	–	13	Ext. Reset Pulse Duration	6.5	–	10.0	–	ns
t_{ptoeen}	B	14	Product Term OE, Enable	–	15.0	–	18.0	ns
$t_{ptoedis}$	C	15	Product Term OE, Disable	–	15.0	–	18.0	ns
t_{goeen}	B	16	Global OE, Enable	–	9.0	–	12.0	ns
t_{goedis}	C	17	Global OE, Disable	–	9.0	–	12.0	ns
t_{wh}	–	18	External Synchronous Clock Pulse Duration, High	5.0	–	6.0	–	ns
t_{wl}	–	19	External Synchronous Clock Pulse Duration, Low	5.0	–	6.0	–	ns

Table 2-0030B/2128-100

1. Unless noted otherwise, all parameters use the GRP, 20 PTXOR path, ORP and Y0 clock.
2. Refer to Timing Model in this data sheet for further details.
3. Standard 16-bit counter using GRP feedback.
4. Reference Switching Test Conditions section.

Internal Timing Parameters[1]

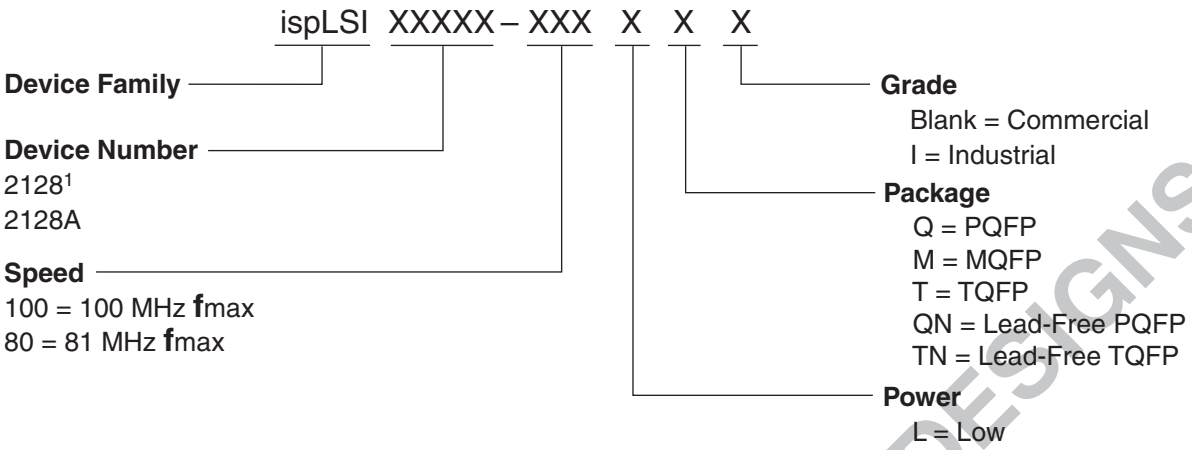
Over Recommended Operating Conditions

PARAMETER	#[2]	DESCRIPTION	-100		-80		UNITS
			MIN.	MAX.	MIN.	MAX.	
Inputs							
t_{io}	20	Input Buffer Delay	–	0.5	–	1.8	ns
t_{din}	21	Dedicated Input Delay	–	2.2	–	4.4	ns
GRP							
t_{grp}	22	GRP Delay	–	1.7	–	2.6	ns
GLB							
t_{4ptbpc}	23	4 Product Term Bypass Path Delay	–	5.8	–	8.1	ns
t_{4ptbpr}	24	4 Product Term Bypass Path Delay	–	5.8	–	6.8	ns
t_{1ptxor}	25	1 Product Term/XOR Path Delay	–	6.8	–	8.0	ns
$t_{20ptxor}$	26	20 Product Term/XOR Path Delay	–	7.3	–	8.8	ns
t_{xoradj}	27	XOR Adjacent Path Delay[3]	–	8.0	–	9.8	ns
t_{gbp}	28	GLB Register Bypass Delay	–	0.5	–	1.3	ns
t_{gsu}	29	GLB Register Setup Time befor Clock	1.2	–	1.4	–	ns
t_{gh}	30	GLB Register Hold Time after Clock	4.0	–	6.0	–	ns
t_{gco}	31	GLB Register Clock to Output Delay	–	0.3	–	0.4	ns
t_{gro}	32	GLB Register Reset to Output Delay	–	1.3	–	1.6	ns
t_{ptre}	33	GLB Product Term Reset to Register Delay	–	6.1	–	8.6	ns
t_{ptoe}	34	GLB Product Term Output Enable to I/O Cell Delay	–	8.6	–	9.0	ns
t_{ptck}	35	GLB Product Term Clock Delay	4.1	7.1	5.6	10.2	ns
ORP							
t_{orp}	36	ORP Delay	–	1.4	–	2.0	ns
t_{orpbp}	37	ORP Bypass Delay	–	0.4	–	0.5	ns
Outputs							
t_{ob}	38	Output Buffer Delay	–	1.6	–	2.0	ns
t_{sl}	39	Output Slew Limited Delay Adder	–	10.0	–	10.0	ns
t_{oen}	40	I/O Cell OE to Output Enabled	–	4.2	–	4.6	ns
t_{odis}	41	I/O Cell OE to Output Disabled	–	4.2	–	4.6	ns
t_{goe}	42	Global Output Enable	–	4.8	–	7.4	ns
Clocks							
t_{gy0}	43	Clock Delay, Y0 to Global GLB Clock Line (Ref. clock)	2.7	2.7	3.6	3.6	ns
$t_{gy1/2}$	44	Clock Delay, Y1 or Y2 to Global GLB Clock Line	2.7	2.7	3.6	3.6	ns
Global Reset							
t_{gr}	45	Global Reset to GLB	–	9.2	–	11.4	ns

Table 2- 0036C/2128-100

1. Internal Timing Parameters are not tested and are for reference only.
2. Refer to Timing Model in this data sheet for further details.
3. The XOR adjacent path can only be used by hard macros.

Part Number Description



1. Discontinued per PCN #02-06. Contact Rochester Electronics for available inventory.

ispLSI 2128/A Ordering Information

Conventional Packaging

COMMERCIAL

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	100	10	ispLSI 2128A-100LQ160	160-Pin PQFP
	100	10	ispLSI 2128A-100LT176	176-Pin TQFP
	81	15	ispLSI 2128A-80LQ160	160-Pin PQFP
	81	15	ispLSI 2128A-80LT176	176-Pin TQFP
	100	10	ispLSI 2128-100LQ[1]	160-Pin PQFP
	100	10	ispLSI 2128-100LT[1]	176-Pin TQFP
	81	15	ispLSI 2128-80LQ[1]	160-Pin PQFP
	81	15	ispLSI 2128-80LT[1]	176-Pin TQFP

1. Discontinued per PCN #02-06. Contact Rochester Electronics for available inventory.

INDUSTRIAL

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2128A-80LT176I	176-Pin TQFP
	81	15	ispLSI 2128-80LTI[1]	176-Pin TQFP

1. Discontinued per PCN #02-06. Contact Rochester Electronics for available inventory.

ispLSI 2128/A Ordering Information (Cont.)

Lead-Free Packaging

COMMERCIAL

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	100	10	ispLSI 2128A-100LQN160	Lead-Free 160-Pin PQFP
	100	10	ispLSI 2128A-100LTN176	Lead-Free 176-Pin TQFP
	81	15	ispLSI 2128A-80LQN160	Lead-Free 160-Pin PQFP
	81	15	ispLSI 2128A-80LTN176	Lead-Free 176-Pin TQFP

INDUSTRIAL

FAMILY	Fmax (MHz)	Tpd (ns)	ORDERING NUMBER	PACKAGE
ispLSI	81	15	ispLSI 2128A-80LTN176I	Lead-Free 160-Pin TQFP

Revision History

Date	Version	Change Summary
—	09	Previous Lattice release.
August 2006	10	Updated for lead-free package options.